Design of a Low Phase Distortion GaAs FET Power Limiter

T. Parra, M. Gayral, O. Llopis, M. Pouysegur, JF. Sautereau, and J. Graffeuil

Abstract—**A simple design technique for a GaAs FET limiter exhibiting minimum phase distortion is presented. The key idea in removing phase distortion by selecting an appropriate device and designing a bias circuit is based on the observed properties of the gate barrier under large-signal conditions. Also presented are some illustrative examples and simulation results. The proposed technique is suitable for MMIC design.**

I. Introduction

Phased array antennas require limiter modules capable of supplying to the receiver signals which do not exceed a given threshold regardless of the level of the incoming signal to the active antenna. A classical implementation for such a function involves p-i-n diodes but is not suitable for building MMIC blocks.

A GaAs MESFET limiter has therefore been introduced [1]. The basic idea is to operate the FET beyond its compression point so that the RF level at its output cannot exceed the saturation level, irrespective of the incoming signal amplitude. The dynamic range can be increased by cascading many devices [1].

The major drawback of this technique is that the phase shift introduced by the limiter depends on the amplitude of the RF signal. Moreover the phase shift variation versus the power level is unpredictable. Therefore the phased array antenna cannot hold this distortion since the phase information conveyed by the signal is lost.

In this paper we first present large-signal phase distortion measurements performed on different GaAs FET's. From an observed correlation between the amplitude of the phase distortion and some of the device electrical parameters, a possible origin is suggested for this phase distortion.

Then, a circuit design technique of reducing phase distortion is proposed. Both large-signal simulations and RF measurements substantiate our proposal.

II. Phase Shift Distortion Measurements and Device Characterization

A. Phase Shift Distortion Measurements

Fig. 1 shows a block diagram of the experimental setup used for large-signal phase distortion measurements. A phase-locked RF generator ($f = 8.1$ GHz) delivers the input signal to the gate of a GaAs FET via an input slide-screw tuner. The device is inserted into a coaxial test jig. An output slide-screw tuner delivers the output power to the matched input of a spectrum analyzer to be sure there is no parasitic oscillation and the harmonic signals are held negligible. A vector network analyzer is used to measure the phase shift between the limiter output and input signals.

The measurements procedure is as follows: First, the two tuners are tuned to get the maximum small-signal power gain. Second, the power is swept from low level to a level slightly beyond saturation and the output tuner match is slightly modified to maintain phase variations at a minimum over the maximum power range beyond saturation.

We thus measured the phase distortion introduced by a set of ten different MESFET devices exhibiting an output power at 1 dB compression in the range of 14 dBm. All these devices were commercially available (Mitsubishi 1402 and Mitsubishi 1412) and were assumed to exhibit identical electrical characteristics since they were all processed in the same way (the lowest noise figure devices being called 1412). However, as depicted in Fig. 2, two different types of phase distortion behavior can be observed: some devices exhibit a phase shift drop when the input power level exceeds 4 dBm; others exhibit a phase shift drop when the input power level exceeds -6 dBm and a phase shift rise beyond a 4 dBm power level.

It is worth pointing out that for an output power level ranging from 5 dBm to 10 dBm, phase distortion $\Delta\Phi$ (see Fig. 2) can be as large as 10° on some devices and as little as 1° on others.

As illustrated in Fig. 3, the phase shift drop, Φ, observed in some devices beyond 4 dBm is associated with a large rise of the dc gate current. To thoroughly understand the different types of phase shift behavior among devices, a static and dynamic comparative electrical characterization was performed.

B. Electrical Characterization

Standard techniques of dc measurements [2] were used to obtain main channel and Schottky gate electrical parameters. Among these parameters (e.g., channel pinch-off voltage, channel resistance, series resistances, gate junction ideality factor, built-in voltage or gate saturation current), a correlation between reverse gate saturation current (I_s) and limiter phase shift variations was observed. Indeed, as shown in Table I for the six more representative devices, an increased I_s corresponds to an increased phase distortion, $\Delta\Phi$.

For each device an equivalent circuit was generated from S parameter measurements (HP 8510) between 50 MHz and 20 GHz. No similar correlation was found between any of the equivalent circuit element values and phase shift variations. Therefore the current results suggest that only those devices that exhibit a small reverse gate saturation current must be used in low phase distortion limiters.

Since the aforementioned devices present a gate section approximately equal to $2.8 \cdot 10^{-6}$ cm^2, a saturation current beyond 40 pA corresponds to a saturation current density beyond approximately $14.3 \cdot 10^{-6}$ A$\cdot$cm^{-2}.

According to the thermoionic emission theory, the reverse saturation current density, J_s, is given by

$$J_s = A^* \cdot T^2 \cdot \exp[-qV_{bi}/nkT]$$

where A^* is the effective Richardson constant, T the temperature, q the electronic charge, n the ideality factor, and V_{bi} the built-in voltage. Therefore a lower J_s corresponds to a higher built-in voltage, and a higher built-in voltage corresponds to the onset of forward gate conduction for a higher gate–source

Manuscript received October 8, 1990; revised January 22, 1991.

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IEEE Log Number 9144284.

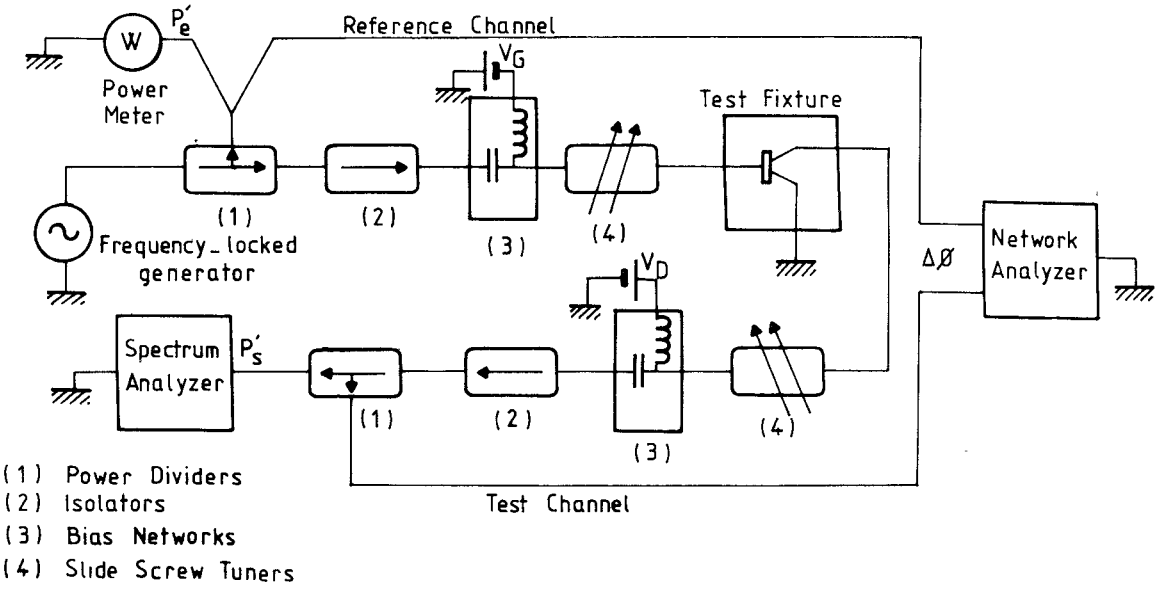

Fig. 1. Experimental setup used for large-signal phase distortion measurements on packaged MESFET's at 8.1 GHz.

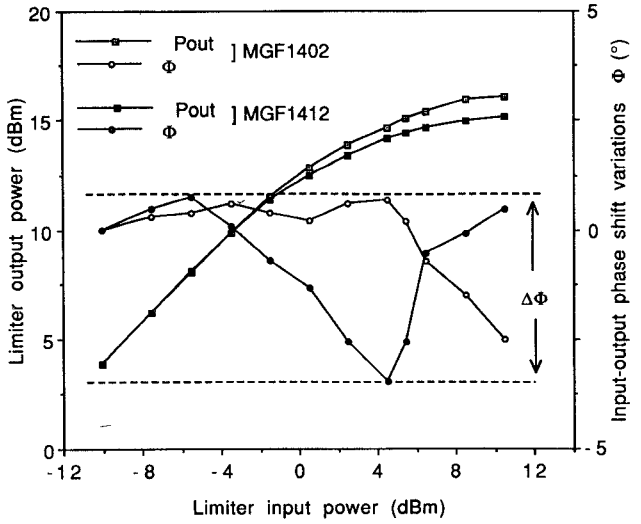

Fig. 2. The two different typically observed output power, P_{out}, and input–output phase shift variations Φ versus input power ($f = 8.1$ GHz). The maximum range $\Delta\Phi$ (also called phase distortion) of the observed variations is pictured as well.

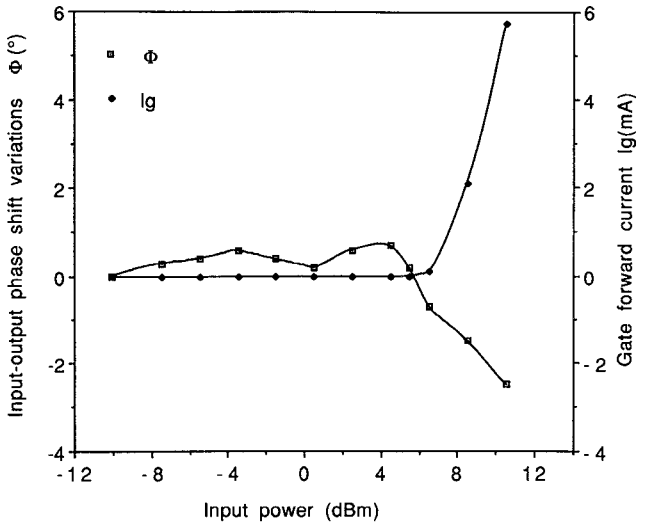

Fig. 3. Simultaneous phase shift variations Φ and forward gate current I_g variations versus input power.

TABLE I
MAIN ELECTRICAL PARAMETERS MEASURED ON THE DIFFERENT MESFET'S INVESTIGATED

Device	MGF1412_2	MGF1412_5	MGF1412_4	MGF1402_6	MGF1402_8	MGF1402_5
$-V_t$(V)	0.76	1.38	1.44	1.12	1.87	1.96
I_{dss} (mA)	34.6	76.5	81.4	56.8	78.1	84.5
$G_{m_{max}}$ (mS)	89.5	82.6	82.4	81.9	71.5	68.7
$-V_{br}$ (V)	15.1	6.5	10.9	11.9	11.2	10.9
I_s (pA)	30	31.4	41.2	92.6	121	132.7
$\Delta\Phi_{min}$(°)	2.7	2.8	4.3	4.4	4.7	4.8
INCREASING PHASE DISTORTION →						

A correlation is highlighted between the gate saturation current, I_s, and the minimum phase distortion in the input power range: −10 dBm to 12 dBm.

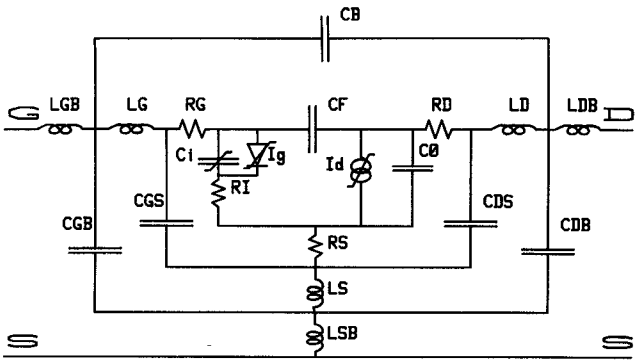

Fig. 4. Large-signal equivalent circuit of a packaged MESFET. Linear elements are obtained from S parameter measurements (40 MHz–20 GHz) and nonlinear elements from pulsed current–voltage and 10 MHz capacitance-voltage measurements.

voltage (as can be seen from the forward current–voltage characteristic of the gate) or, similarly, a higher input power. This corroborates the Fig. 3 results, which relate the phase shift drop to the forward gate current increase.

Still to be investigated is why forward gate conduction increases the phase shift distortion.

III. Large-Signal Simulations

The simulator used (LIMHA, developed by IRCOM Limoges [3]) is based on the harmonic balance method.

We used the nonlinear model presented in Fig. 4. Among the classical nonlinear models [4]–[10] we chose a Tajima [6] drain current expression $I_d = fct(V_{gs}, V_{ds})$ and a polynomial one for the input capacitance $C_i(V_{gs}, V_{ds})$. The drain current is obtained from pulse measurements to prevent any thermal or trapping problems [11], [12]. The nonlinear input capacitance, C_i, is measured at 10 MHz using an impedance analyzer and the linear parameters of the model are obtained from static and S parameter characterizations.

From this model, a simulation of the limiter inserted between matched terminations is performed. The simulated phase variations displayed in Fig. 5 are in good qualitative agreement with experimental results.

Finally, the nonlinear input gate–source capacitance of the model was replaced in the simulation by a constant input capacitance. As shown in Fig. 6, simulated phase shift variations are fully canceled for an input power below 2 dBm if the input capacitance is held constant. Hence it can be stated that the nonlinear input capacitance is responsible for most of the phase shift variations at moderate power levels.

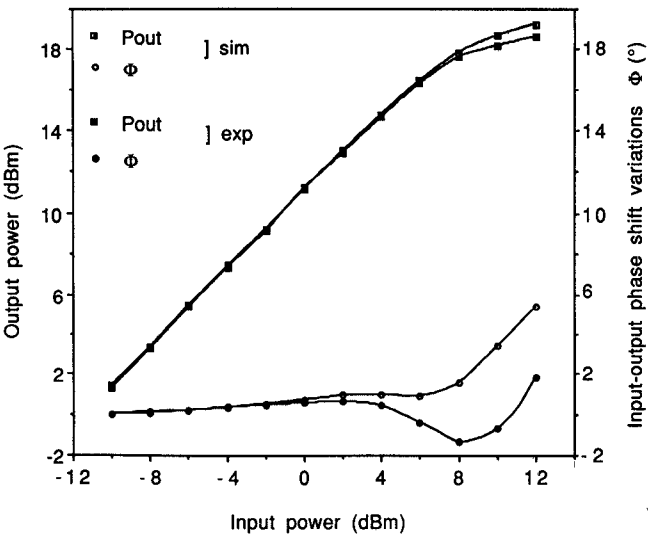

Fig. 5. Measured ("exp") and simulated ("sim," harmonic balance) output power P_{out} and phase shift variations Φ versus input power (matched terminations and $f = 8.1$ GHz).

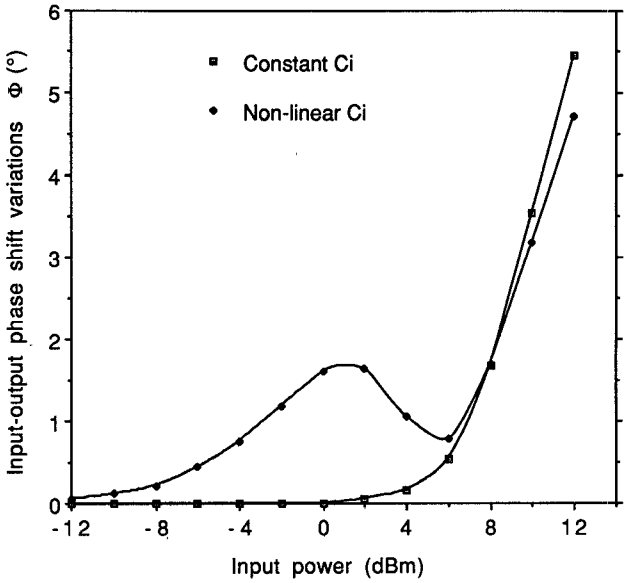

Fig. 6. Simulated phase shift variations Φ using either a nonlinear input capacitance C_i or a constant (small-signal value) capacitance. It appears that the nonlinear C_i is responsible for most of the large-signal phase shift variations observed at moderate input power levels (below 2 dBm).

IV. Discussion and Conclusion

Given the results already reported, we suggest that phase shift variations are mostly related to large input capacitance variations occurring during a fraction of the RF cycle when the gate becomes forward biased.

Therefore, to prevent phase distortion caused by forward gate conduction at moderate input power level, the addition of an external series resistor, R_g, in the bias gate voltage supply (Fig. 7) is suggested.[1] Thus, at the onset of forward conduction, the voltage drop across that resistor increases the reverse gate–source voltage. Hence, for a given input power, the fraction of the RF cycle corresponding to a forward-biased gate is smaller and the variations of the gate capacitance also diminish.

Fig. 8(a) shows that the simulated phase shift variations decrease as soon as the value of the self-bias resistor, R_g, is correctly set. In practice, a good approximation was found for R_g, that is,

$$R_g = R_0 \cdot (400/Z)$$

where Z is the gate width in micrometers and R_0 is equal to 20 Ω. Fig. 8(b) shows that the measured phase variations obtained using the proposed technique are now less than 2° for an input power range of 22 dB.

[1]Patent pending.

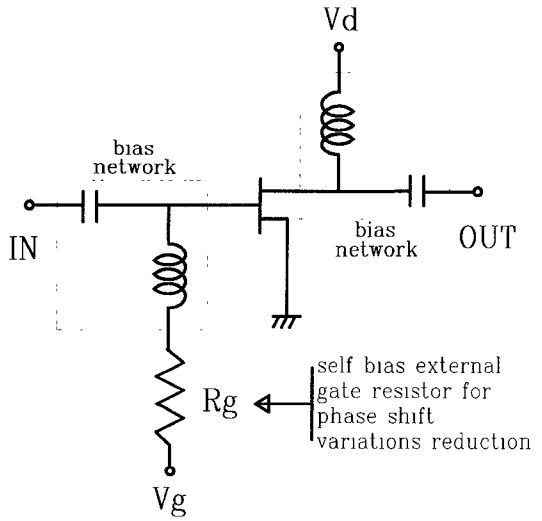

Fig. 7. Implementation of a self-bias gate resistor R_g in the bias network for phase distortion minimization.

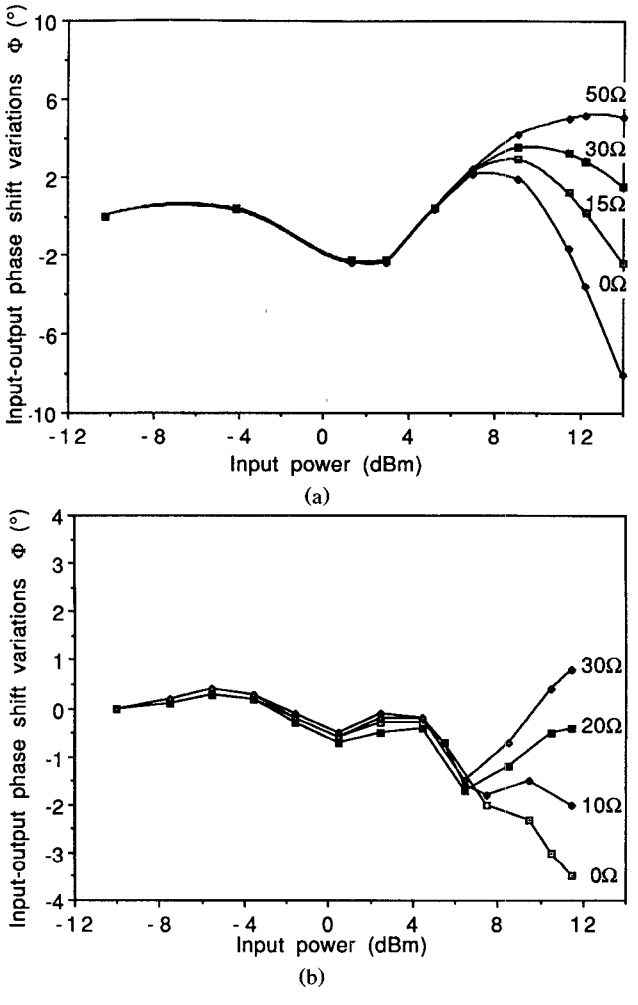

Fig. 8. (a) Simulated phase shift variations Φ versus input power with the value of the self-bias resistor R_g as parameter. A value of R_g in the 20 Ω range provides the lowest phase distortion for the considered device. (b) Measured phase shift variations Φ versus input power for different values of the self-bias gate resistor R_g. As predicted by simulations, a value for R_g near 20 Ω provides the lowest phase distortion.

To conclude, it may be stated that low phase distortion GaAs MESFET limiters can be designed provided that the FET used in the limiter features a gate built-in voltage as large as possible (a correct value is in excess of 0.75 V, which is classical for GaAs FET) and that a self-bias gate series resistor is used at an appropriate value. These two conditions can be easily satisfied, especially in MMIC implementations.

Acknowledgment

The authors would like to thank S. Bertrand (Alcatel Espace) for suggesting this work, L. Lapierre (CNES) and M. Camiade (Thomson-DHM) for their authorization to use some of their characterization tools, and J. Rayssac for technical assistance.

References

[1] S. Bertrand, "Amplificateur-limiteur à TEC sans déphasage. Applications dans la bande 7.9–8.4 GHz," *Journées Nationales Micro-ondes de Nice*, 1987, pp. 146–147, June 1987.
[2] H. Fukui, "Determination of the basic device parameters for a GaAs MESFET," *Bell Syst. Tech. J.*, vol. 58, no. 3, Mar. 1979.
[3] M. Gayral *et al.*, "A general method for the analysis of non linear microwave circuits," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1987, pp. 119–121.
[4] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuit," *Trans. Microwave Theory Tech.*, vol. MTT-28, May 1980.
[5] W. R. Curtice, "A non-linear GaAs FET model for use in the design of output circuit for power amplifiers," *Trans. Microwave Theory Tech.*, vol. MTT-33, Dec. 1985.
[6] Y. Tajima, "GaAs FET large signal model and its application to circuit design," *IEEE Trans. Electron Devices*, vol. ED-28, Feb. 1981.
[7] A. Materka, "Computer calculation of large signal GaAs FET amplifier characteristic," *Trans. Microwave Theory Tech.*, vol. MTT-33, Feb. 1985.
[8] H. Statz, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. Electron Devices*, vol. ED-34, Feb. 1987.
[9] I. Telliez, B. Carnez, M. Gayral, and C. Rumelhard, "Modélisation grand signal de TEC pour la simulation de Circuits Intégrés Monolithiques Hyperfréquences en GaAs," *Journées Nationales Micro-ondes de Nice*, pp. 230–232, June 1987.
[10] J. W. Bandler, "A unified framework for harmonic balance simulation sensitivity analysis," in *IEEE MTT-S Int. Microwave Dig.*, June 1988.
[11] M. Paggi, "Nonlinear GaAs MESFET modelling using pulsed gate measurement," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1988.
[12] J. F. Vidalou, "On-wafer large signal pulsed measurements," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1989, pp. 831–834.

An Approach to Microwave Imaging Using a Multiview Moment Method Solution for a Two-Dimensional Infinite Cylinder

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Abstract—**An approach based on a multiview solution to the inverse-scattering problem of a two-dimensional infinite cylinder is developed in a space–frequency domain. Microwave imaging is simulated by a com-**

Manuscript received May 10, 1990; revised December 3, 1990.
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IEEE Log Number 9042498.